REMARKS

Attached hereto is a marked-up version of the changes made to the specification and claims by the current preliminary amendment. The attached page is captioned "**Version With Markings to Show Changes Made.**"

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Specification:

Paragraph beginning at line 4 of page 2 has been amended as follows:

With respect to data retrieving operations, packets received from a communication system or read from local storage are required to be de-packetized before processing by each respective data processor. The de-packetization process includes, first, detection of the sync-word, followed by verification of the packet ID, extraction of timing and necessary side information, determining the payload size and, finally, extraction and concatenation of the payload to reconstruct the data. The de-packetized data may be passed to a data processor for further processing. For example, the data processor for MPEG compressed audio data will be a corresponding MPEG audio decoder; furthermore, this audio decoder may be implemented using programmable DSP (Digital Signal Processor).

Paragraph beginning at line 13 of page 10 has been amended as follows:

Figure 2 is a block diagram of a conventional circuit for de-packetizing and processing data;

Paragraph beginning at line 15 of page 10 has been amended as follows:

Figure 3 is a block diagram of an embodiment of a device for ~~practising~~practicing the present invention;

Paragraph beginning at line 19 of page 10 has been amended as follows:

Figure 5 is a flow ~~charge~~chart illustrating an embodiment of part of the de-packetizing process according to the present invention.

Paragraph beginning at line 21 of page 11 has been amended as follows:

Figure 4 illustrates in more detail an embodiment of a device for de-packetizing and aligning input data according to the present invention. A packetized data source (not shown)

is connected to a Data Input Interface 401 which provides necessary ~~signallingsignaling~~ for the external packetized data source as well as possible format conversion. For example, the data input interface may be an embodiment of a serial-to-parallel ~~adaptiveadaptor~~ which converts serial format data such as the I2S format to parallel data. The Data Input Interface 401 is coupled to an Input FIFO 402.

In the Claims:

Claims 1-29 have been amended as follows:

1. (Amended) An ~~A~~apparatus for depacketizing and aligning packetized input data, ~~comprising~~comprising:

an input memory for receiving, storing, and output of the input data, and for outputting of units of a payload of a data packet of the input data;

data processing means for receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet and generating a payload size signal indicative of the size of the payload, and for separately receiving and effecting data processing of the payload;

a word formatter for receiving said units of said payload outputted from the input memory, gathering and aligning said units to form data words, and outputting said words;

a payload counter for controlling the input memory in accordance with the payload size signal ~~whereby~~and configured to cause the payload units to be outputted from the input memory to the word formatter; and

an input buffer for receiving said data words from the word formatter and storing these, and for transferring the data words to the data processing means, to effect said separate receiving of said payload;

said data processing means for effecting said data processing using the received said data words.

2. (Amended) The ~~A~~apparatus ~~as claimed in~~of claim 1 having a data input interface through which the input data is transferred to the input memory, said data input interface ~~for performing~~configured to perform hand shaking with a packetized data source of said input data.

3. (Amended) The ~~A~~apparatus ~~as claimed in~~of claim 1 ~~or claim 2~~ wherein the input memory has a fullness level detector for generating a level-filled signal when the input data received thereby is such as to fill the input memory to a predetermined level, and said data processing means is responsive to generation of said level-filled signal to execute said receiving the outputted input data from the input memory and detecting, identifying, and determining payload size of the data packet and generating said payload size signal.

4. (Amended) The ~~A~~apparatus ~~as claimed in~~of claim 3, ~~having~~comprising an interrupt controller~~,~~ for receiving said level-filled signal and generating an interrupt signal pursuant to receipt thereof, said data processing means ~~being~~ arranged for receipt of said interrupt signal and, on receipt thereof, for executing said receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet therein and generating said payload size signal.

5. (Amended) The ~~A~~apparatus ~~as claimed in claim 3 or~~of claim 4~~, as appended directly or indirectly to claim 2,~~ wherein the input memory has a further fullness level detector for generating and directing to said data input interface a further level-filled signal when the input thereto of fresh input data is such as to fill the input memory to a further predetermined level, said data input interface ~~being~~ responsive to receipt of said further level-filled signal to generate a data request signal for direction to said packetized data source~~,~~ indicating of a need to modify the data transmission rate of the input data directed to the apparatus from the packetized data source.

6. (Amended) The Aapparatus ~~as claimed in any preceding~~of claim 1 wherein the input memory is controlled whereby said input data comprising said packet is removed from the input memory and relaced by fresh input data, pursuant to the transfer to the data processing means of said words representing the data packet to the data the apparatus being arranged for repetitive depacketizing and aligning of data packets and data processing thereof, the data processing means being arranged for repetitively and alternatingly executing a step comprising said receiving the outputted input data from the input memory and detecting, identifying and determining payload size of the data packet therein and generating said payload size signal, and ~~a step~~ comprising ~~said~~ separating receiving and effecting data processing of the payload of the data packet.

7. (Amended) The Aapparatus ~~as claimed in any preceding~~of claim 1 wherein the data processing means includes a digital signal processor, data/program memory, DMA controller and input buffer, each in data communication via a bus.

8. (Amended) The Aapparatus ~~as claimed in~~of claim 7~~,~~ wherein the word formatter is arranged for generating a DMA request signal when a said data word is formed thereby, and the DMA controller is responsive to said DMA request signal to generate and direct a transfer signal to the digital signal processor, the digital signal processor being responsive to the transfer signal to enable the DMA controller to move the data word from the word formatter to the input buffer for subsequent processing.

9. (Amended) The Aapparatus ~~as claimed in~~of claim 5 wherein said input memory is a first in first out memory.

10. (Amended) The Aapparatus ~~as claimed in any preceding~~of claim 1 wherein the data processing means is arranged to execute said detecting and identifying the data packet by detection of a sync-word, followed by verification of the packet ID.

11. (Amended) The Aapparatus ~~as claimed in any preceding~~of claim 1 wherein the data processing means, pursuant to said detecting and identifying the data packet, extracts timing information from the input data.

12. (Amended) The Aapparatus ~~as claimed in any preceding~~of claim 1 wherein the data processing means, pursuant to said detecting and identifying the data packet, extracts side information from the input data.

13. (Amended) A method for depacketizing and aligning packetized input data, comprising:

receiving and storing the input data in an input memory;

outputting the stored input data to data processing means;

by use of the data processing means, detecting, identifying and determining the size of a payload of a data packet of the input outputted thereto;

by use of the data processing means, generating a payload size signal indicative of the size of the payload;

controlling the input memory in accordance with the payload size signal ~~whereby~~ to cause payload units ~~which~~that form said payload to be outputted from the input memory to the word formatter;

by use of said word formatter, gathering and aligning said payload units outputted thereto to form data words;

outputting said data words from said word formatter to an input buffer and storing these in said input buffer;

transferring said data words to the data processing means; and

effecting data processing on the data packet represented by the data words transferred thereto~~,~~ using the transferred data words.

14. (Amended) ~~A~~The method ~~as claimed in~~of claim 13 wherein the input data is transferred to the input memory via ~~an~~a data input interface ~~which~~that performs hand shaking with a packetized data source of said input data.

15. (Amended) ~~A~~The method ~~as claimed in~~of claim 13 ~~or claim 14 including the step of~~comprising generating a level-filled signal when the input data received by the input memory is such as to fill the input memory to a predetermined level, and causing said data processing means to effect said detecting, identifying, and determining payload size of the data packet, and to said generate payload size signal, pursuant to generation of the level-filled signal.

16. (Amended) ~~A~~The method ~~as claimed in~~of claim 13, ~~including the step of~~comprising generating an interrupt signal from said level-filled signal and directing said interrupt signal to said data processing means to cause said data processing means to effect said receiving the outputted input data from the input memory and detecting, identifying, and determining payload size of the data packet therein and to generate said payload size signal.

17. (Amended) ~~A~~The method ~~as claimed in~~of claim 15, ~~or claim 16, as appended directly or indirectly to claim 14, including the step of~~comprising generating and directing to said data input interface a further level-filled signal when the input thereto of fresh input data is such as to fill the input memory to a further predetermined level, and causing said data input interface to generate, responsive to receipt thereby of said further level-filled signal, a data request signal for direction to said packetized data source, indicative of a need to modify the data transmission rate of the input data directed to the apparatus from the packetized data source~~,~~.

18. (Amended) ~~A~~The method ~~as claimed in any one of claims 13 to 17~~of claim 13 wherein the input memory is controlled whereby said input data comprising a said packet is removed from the input memory and relaced by fresh input data pursuant to the transfer of said data words representing that data packet to the data processor, and ~~wherein a step~~

compromising ~~said~~ receiving the outputted input data from the input memory and detecting, identifying, and determining payload size of the data packet therein and generating said payload size signal indicative of the size of the payload, and ~~a step~~ comprising effecting data processing of the payload are repetitively and alternatingly executed.

19. (Amended) ~~A~~The method ~~as claimed in~~of claim 18, ~~including~~comprising generating a DMA request signal when a said data word is formed, and applying the DMA request signal to a digital signal processor forming part of said data processing means to cause the digital signal processor to enable a DMA controller to move that data word from the word formatter to an input buffer of the data processor for subsequent processing.

20. (Amended) ~~A~~The method ~~as claimed in any one of claims 13 to 19~~of claim 13 wherein said input memory is a first in first out memory.

21. (Amended) ~~A~~The method ~~as claimed in any one of claims 13 to 20~~of claim 13 wherein the data processing means executes said detecting and identifying the data packet by detection of a sync-word, followed by verification of the packet ID.

22. (Amended) ~~A~~The method ~~as claimed in any one of claims 13 to 21~~of claim 13 wherein the data processing means extracts timing information from the input data pursuant to said detecting and identifying the data packet.

23. (Amended) ~~A~~The method ~~as claimed in any one of claims 13 to 22~~of claim 13 wherein the data processing means extracts side information from the input data pursuant to said detecting and identifying the data packet.

24. (Amended) An ~~A~~apparatus for depacketizing and aligning packetized input data, ~~having~~comprising:

an input memory for receiving, storing, and output of the input data, and for outputting of units of a payload of a data packet of the input data;

data processing means for receiving the outputted input data from the input memory and detecting, identifying, and determining payload size of the data packet and generating a payload size signal indicative of the size of the payload, and for separately receiving and effecting data processing of the payload;

a word formatter for receiving said units of said payload outputted from the input memory, gathering and aligning said units to form data words, and outputting said words;

a payload counter for controlling the input memory in accordance with the payload size signal whereby to cause the payload units to be outputted from the input memory to the word formatter; and

means for transferring the data words to the data processing means~~,~~ to effect said separate receiving of said payload.

25. (Amended) A method for depacketizing and aligning packetized input data comprising:

receiving and storing the input data in an input memory;

outputting the stored input data to data processing means;

by use of the data processing means, detecting, identifying, and determining the size of a payload of a data packet of the input data outputted thereto;

by use of the data processing means, generating a payload size signal indicative of the size of the payload;

controlling the input memory in accordance with the payload size signal ~~whereby~~ to cause payload units ~~which~~that form said payload to be outputted from the input memory to the word formatter;

by use of said word formatter, gathering and aligning said payload units outputted thereto to form data words;

outputting said data words from said word formatter to an input buffer and storing these in said input buffer;

transferring said data words to the data processing means.

26. (Amended) An ~~A~~apparatus for ~~depacketising~~depacketizing and aligning ~~packetised~~packetized input data, ~~including~~comprising data processing means ~~which in use detects~~configured to detect a payload of a data packet in the input data and ~~processes~~to process the payload.

27. (Amended) The ~~A~~apparatus ~~as claimed in~~of claim 26 wherein the data processing means repetitively and alternatingly executes functions of detecting and processing payloads ~~and processing these~~.

28. (Amended) A method for depacketizing and aligning packetized input data, ~~wherein functions of~~comprising: detecting a payload of a data packet in the input data and processing the payload ~~are effected~~ separately by the same data processing means.

29 (Amended) ~~A~~The method ~~as claimed in~~of claim 28, wherein said functions are repetitively and alternatingly executed with respect to successive data packets in the input data.